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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,095	12/11/2003	Wang-Jin Chen	250606-1020	9153

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THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,095	CHEN ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/733,095 filed 12/11/2003.

2. Claims 1-16 are pending in the Application.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: it is not clear (claims 1, 6 and 13) what the relationships between the "placement direction of the head section and the tail section" with the orientation of the I/O circuit itself. It's read as the placement direction of the I/O circuit is perpendicular to itself. Moreover the Specification, particularly, page 3, does not clarify the problem.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 5-7, 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Ali et al. (US Patent 6,836,026).

With respect to claims 1, 6 Ali et al. teaches an I/O circuit placement method for placing I/O circuits included in a semiconductor device, a semiconductor device (abstract), comprising a step of: placing at least two rows of I/O circuits on a first side of a chip as shown on the Fig. 7, there are two rows in a layout of an IC design as first I/O region 62 and second I/O region 68 (col. 10, ll.9-14), i.e. multiple I/O cells may be placed in multiple rows (col. 10, ll.53-55), wherein each I/O circuit has a head section and a tail section, the placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the rows as shown on the Figs 1 and 2, wherein a lateral dimension of the I/O cells in a direction perpendicular to the outer lateral edge of the die (col. 6, ll.9-11).

With respect to claim 13 Ali et al. teaches a semiconductor device (abstract), comprising: a chip as shown on the Fig. 7 (col. 4, ll.41-48); a core circuit region disposed on the chip (col. 4, ll.48-53); a loop of I/O circuits disposed at the periphery of the chip and around the core circuit region as shown on the Fig. 7 there are two rows in a layout of an IC design as first I/O region 62 and second I/O region 68 (col. 10, ll.9-14), i.e. multiple I/O cells may be placed in multiple rows (col. 10, ll.53-55); and at least one row of I/O circuits disposed between the loop of I/O circuits, wherein each I/O circuit has a head section and a tail section, the placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the loop or the row as shown on the Figs 1 and 2, wherein a lateral dimension of the I/O cells in a direction perpendicular

to the outer lateral edge of the die (col. 6, ll.9-11), wherein the lateral dimensions of the I/O devices might be in the direction perpendicular to the outer lateral edge depending on the relationship of the length and width of the I/O devices (col. 6, ll.23-30).

With respect to claims 2, 5, 7, 11, 12 Ali et al. teaches:

Claims 2 and 7: a step of placing another row of I/O circuits on a second side of the chip as shown on the Fig. 7 as second I/O region 68 (col. 10, ll.9-14), i.e. multiple I/O cells may be placed in multiple rows (col. 10, ll.53-55);

Claims 5,12: a different number of I/O circuits are placed in different rows (col. 8, ll.27-30);

Claim 11: a core circuit region disposed on the chip, wherein the rows of I/O circuits are disposed outside the core circuit region and are at the periphery of the chip as shown on the Fig. 7 (col. 4, ll.48-55).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 4, 8-10, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ali et al. (US Patent 6,836,026).

With respect to claims 3, 4, 8-10, 14-16 Ali et al. teaches the limitations from which the claims depend, additionally:

Claims 3, 4, 8-10, 14-16 the head sections are oriented to the tail sections in the adjacent rows; the head sections are oriented to the head sections in the adjacent rows; the tail sections are oriented to the tail sections in the adjacent rows as shown on the Figs. 1, 2 and 7, wherein placement of the I/O cells on the flip chip (col. 4, ll.47-48) depends on the dimensions of the I/O cells (length and height) (col. 6, ll.9-11; ll.20-29), wherein designer use I/O cells that are designed for I/O limited IC for core limited designs (col. 9, ll.67; col. 10, ll.1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made, that I/O cells might be oriented in any direction using the technique of designing I/O limited IC (col. 2, ll.53-54) without die area waste (col. 4, ll.33-38), since the direction of the I/O cells depends on the its dimensions (length and height) (col. 6, ll.9-11; ll.15-23).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER